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10/087,610	03/01/2002	Richard A. Nichols	100.152US01	7953

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EXAMINER	
WONG, LINDA	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,610	NICHOLS, RICHARD A.	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-10,12,13,15,17,21,22,24-26,28 and 30-34* is/are rejected.

7)☒ Claim(s) *6,7,11,14,16,18-20,23,27 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/1/2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, several of the aspects of the invention described below should be added or canceled from the claim(s).

   a. Based on the specifications, the processor can be a component of or coupled to the PLL. (Page 4, paragraph [0042], lines 1-2) The claims recite that the processor is coupled to the oscillator, but Fig. 2 does not show that the processor is coupled to the oscillator.

   b. The specifications also state that the processor analyzes the output from the low pass filter and temperature sensor. (Page 5, paragraph [0051], lines 1-2) Inputs from the LPF and temperature sensor to the processor are not shown in Fig. 2.

   c. The specifications states that the processor produces a holdover control signal to the frequency synthesizer in the oscillator. (Page 5, paragraph [0046], lines 1-4) In Fig. 2, the processor produces an output signal to the PLL but does not show the frequency synthesizer in the oscillator receiving information from the processor. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not

be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims** 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura (US Patent No.: 6542039) in view of Irwin (US Patent No.: 6065140).

   a. **Claim 1**, Ogura discloses a phase comparator having a reference clock signal and feedback signal as received signals (Fig. 1, labels reproduction signal and output from oscillator), a loop filter having an error signal as an input (Fig. 1, label 9), an oscillator receiving a control signal and providing a timing signal as a feedback signal (Fig. 1, label 10 and output from oscillator) and multiple memory blocks or holding means holding instructions indicative of the quality of error level of the reference

clock signal, used for selectively placing the PLL in holdover. (Fig. 1, labels 7a-7d, phase and frequency error signal, Col. 4, lines 7-19, lines 35-48, Col. 5, lines 33-41 and Col. 12, lines 41-55) Although Ogura does not disclose a processor and machine-readable medium, Irwin discloses a central processing unit (CPU), inherently containing a machine readable medium used to contain instructions (Fig. 5, label 110), coupled to the oscillator and receiving a status message (Fig. 5, labels 116 and 106) It would be obvious to one skilled in the art to use the CPU disclosed by Irwin replacing the holding means disclosed by Ogura to perform the functions of analyzing the status message and controlling placing the PLL in holdover to provide a more flexible and prevent quick or slow locking of the PLL.

b. **Claim 2,** Ogura discloses instructions or phase errors stored in the holding means (Fig. 1, labels 7a-7d), which command the phase controlling loop filter to lock or unlock the PLL (Fig. 1, labels 7a-7d and Col. 5, lines 46-54) causing the processor (Fig. 1, labels 8 and 9) to selectively place the PLL in holdover in response to the status message or phase/frequency error. (Col. 12, lines 59-63, Col. 13, lines 54-67 and Col., lines 1-6)

c. **Claim 3**, Ogura discloses instructions or phase errors stored in the holding means (Fig. 1, labels 7a-7d), which command the phase controlling loop filter to lock or unlock the PLL (Fig. 1, labels 7a-7d and Col. 5, lines 46-54) causing the processor (Fig. 1, labels 8 and 9) to

place the PLL in holdover condition if the quality level of the phase/frequency error or status message is less than expected. (Col. 12, lines 41-64, Col. 13, lines 54-67 and Col. 14, lines 1-7)

3. **Claims 4, 5, 8, 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura (US Patent No.: 6542039) in view of Irwin (US Patent No.: 6065140) and further in view of Wesolowski (US Patent No.: 6356156).
   a. **Claim 4** inherits all the limitations of claim 1, but neither Ogura nor Irwin discloses selecting a reference clock signal. Wesolowski discloses selecting the reference clock signal. (Fig. 1, labels 18, 20, and 25) It would be obvious to one skilled in the art to combine Ogura, Irwin and Wesolowski's invention to minimize transfer of wander and jitter from the reference signal. (Col. 1, lines 66-67 and Col. 2, line 1)
   b. **Claim 5** inherits all the limitations of claim 1 and 2.
   c. **Claim 8** inherits all the limitations of claim 3.
   d. **Claim 9** inherits all the limitations of claim 4 and 8.

4. **Claims 10, 12, 13, 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura (US Patent No.: 6542039) in view of Irwin (US Patent No.: 6065140) and further in view of Matsuoka et al. (US Patent No.: 5555247).
   a. **Claim 10** inherits all the limitations of claim 1, but claim 1 does not recite a receiver and a framer. Although Ogura and Irwin does not teach a

receiver and a framer, Matsuoka et al disclose a receiver coupled to receive communication signals (Col. 1, lines 17-20 and Fig. 1, label 41) and for recovering clock and data signals and a status message (Fig. 2, label 47, 45, and 53 respectively) and a framer for locating a frame pulse (Fig. 4, label 110 and Col. 14, lines 29-50) and generating a reference clock signal (Fig. 4, label 110) from the recovered clock (Fig. 4, label 112) and data signals (Fig. 4, label 101). It would be obvious to one skilled in the art to incorporate a PLL with a receiver and framer recited by Matsuoka et al with Ogura's invention to improve the degree of stability for receiving information in a receiver. (Col. 4, lines 31-39)

b. **Claim 12** inherits all the limitations of claims 8 and 10.

c. **Claim 13** inherits all the limitations of claim 8.

d. **Claim 15** inherits all the limitations of claims 1 and 10.

5. **Claims 17, 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura (US Patent No.: 6542039) in view of Irwin (US Patent No.: 6065140).

a. **Claim 17**, Ogura discloses a timing signal generated from a reference clock signal (Fig. 1, label reproduction clock and reproduction signal), monitoring a status message indicative of the quality level (Fig. 1, output from phase error detector, Col. 5, lines 45-54 and Col. 12, lines 41-63), placing the PLL in holdover if the quality level is below a target level (Col. 12, lines 41-64, Col. 13, lines 54-67 and Col. 14, lines 1-7) It would be

obvious to one skilled in the art to perform high-speed and stable phase locking. (Col. 1, lines 33-34).

b. **Claim 21** inherits all the limitations of claim 8.

6. **Claims 22, 24-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura (US Patent No.: 6542039) in view of Irwin (US Patent No.: 6065140) and further in view of Wesolowski (US Patent No.: 6356156).

a. **Claim 22** inherits all the limitations of claim 17, but Ogura does not recite a selection of the reference clock signal. Although Ogura does not teach a selection of the reference clock signal, Wesolowski discloses selecting the reference clock signal. (Fig. 1, labels 18, 20, and 25) It would be obvious to one skilled in the art to combine the admitted prior art, Ogura and Wesolowski's invention to minimize transfer of wander and jitter from the reference signal. (Col. 1, lines 66-67 and Col. 2, line 1)

b. **Claim 24**, Ogura, inherently, disclose holding the PLL for a time depending on the quality level or phase error is at or above a target level. (Fig. 7, Col. 12, lines 41-64, Col. 13, lines 54-67 and Col. 14, lines 1-7)

c. **Claim 25** inherits all the limitations of claim 24.

7. **Claims 26, 28, 30-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura (US Patent No.: 6542039) in view of Irwin (US Patent No.: 6065140).

a. **Claim 26**, Ogura discloses when the quality level of a status message is at or above a target level (Fig. 7, Col. 12, lines 41-64, Col. 13, lines 54-67 and Col. 14, lines 1-7), generating a first error signal (Fig. 1, output from phase error detector), filtering a first error signal (Fig. 1, label 9), generating a timing signal (Fig. 1, label reproduction clock), deriving a first feedback signal (Fig. 1, label reproduction clock). The process stated above is processed again for a second reference signal (Fig. 1, label reproduction clock signal) if the first reference signal is below a target level (Fig. 7), and the second reference signal is at or above the target level (Fig. 7). If either of the reference clock signals is below the target level, the PLL is placed in holdover (Col. 12, lines 41-67, Col. 13, lines 54-67, and Col. 14, lines 1-6) and a timing signal is generated (Fig. 1, label reproduction clock signal).

b. **Claim 28** inherits all the limitations of claim 26.

c. **Claim 30** inherits all the limitations of claim 17.

d. **Claim 31** inherits all the limitations of claim 8.

e. **Claim 32** inherits all the limitations of claim 32.

f. **Claim 33** inherits all the limitations of claims 26 and 1.

g. **Claim 34** inherits all the limitations of claims 33 and 1.

Allowable Subject Matter

8. **Claims 6, 7, 11, 14, 16, 18-20, 23, 27, 29** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LW

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